News Release

Waltham, MA,

CARBON BREAKS SW VALIDATION BARRIER

Replay™ Solves Software Validation Bottleneck for Iterations through Previously Validated Code

WALTHAM, MA – May 18, 2007 - Carbon Design Systems — the leading supplier of tools for the automatic creation, validation, and deployment of virtual hardware models, announced today that it has joined the MIPS Alliance Program (MAP), adding MIPS Technologies, (NASDAQ: MIPS) to its growing number of strategic partners. Carbon also announced that it has integrated its models with the MIPSsim™ Instruction Set Simulator and software debugger to provide a complete validation solution for MIPS-Based™ SoC design. The MIPS32® and MIPS64® RISC microprocessor architectures are industry standards and performance leaders within the embedded industry.

The alliance program collaboration between Carbon and MIPS enables their customers to rapidly identify and fix bugs in both hardware and software. "We're extremely pleased with the joint Carbon/MIPS solution," remarked Jim O'Connor, senior vice president of engineering at iVivity. "This integration has enabled us to identify a number hardware and software bugs in our next-generation SoC. The 100% model visibility and fast runtime capability have enabled us to find and repair bugs five times faster than with our previous FPGA prototype methodology."

"The combination of Carbon's model generation technology with our simulation technology enables our customers to start with system-level development and debug much earlier," noted Jack Browne, vice president of marketing at MIPS Technologies. "This integration enables a system-level approach to validate customer and third-party IP with our industry standard architecture."

"Our collaboration with MIPS will enable our customers to start their system integration tasks even earlier than was previously possible," remarked Rick Lucier, CEO of Carbon Design Systems. "Pre-silicon system integration allows our joint customers to identify and fix problems early in the design cycle, and greatly reduce the amount of time required to bring up the system in the lab. It's win-win solution when we can help our customers reduce costs and increase time-to-revenue."

About The Integration

Carbon software compiles Verilog™ and/or VHDL hardware descriptions into high speed software models. As part of its collaboration with MIPS Technologies, Carbon has developed SystemC technology to link these Carbon models directly to the MIPSsim instruction set

simulator and software debugger. This direct integration allows the entire SoC to be quickly modeled and run in SystemC. The MIPSsim instruction set simulator executes the embedded firmware and generates transactions for the hardware models. Carbon's integration targets these transactions to the correct hardware component and executes the RTL behavior. Software developed and tested on the joint Carbon/MIPS model can be easily debugged, while hardware problems can be quickly diagnosed using Carbon's 100% design visibility, interactive API and VCD/FSDB waveform capability. The ability to concurrently debug hardware and software enables issues to be identified and repaired much more quickly than with any other solution.

Availability

Carbon SOC-VSP software with virtual hardware model generation for MIPS Technologies' MIPSsim instruction set simulator is now publicly available. Call Carbon for product evaluations and pricing. MIPSsim is available from MIPS Technologies today.

About Carbon

Carbon is delivering a high-performance virtual system prototyping solution that enables an ASIC or SoC prototype to be rapidly assembled and functionally validated on an engineer's desktop months before silicon. Carbon's new software approach allows multiple levels of abstraction to be validated together including processors, peripherals, C, SystemC, Verilog, VHDL, IP cores, and transaction-level models. The key to VSP is silicon accuracy and performance -- the ability to execute billions of cycles and boot embedded operating systems, all with desktop software. Problems can be found and resolved during the design cycle -- rather than waiting for idealized behavioral models to be developed or first silicon to be delivered.

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